SILICON RF-GCMOS IC TECHNOLOGY FOR RF MIXED-MODE WIRELESS APPLICATIONS

Jun Ma, Han-Bin Liang, David Ngo, Eddie Spears, Bruce Yeung, Becky Courson, Dan Spooner, Dan Lamey, Julia Alvarez, Tammie Teraji, Jenny Ford, and Sunny Cheng

Communication Products Laboratory
Semiconductor Products Sector
Motorola, In.
2200 W. Broadway Rd., MD M360, Mesa, AZ 85202

ABSTRACT

A submicron silicon *Radio Frequency Graded-Channel MOS* (RF-GCMOS) IC technology has been developed for wireless communication applications. The technology is based on a low power, low cost GCMOS VLSI technology with fully integrated passive components and optimized GC-MOSFETs for RF mixed-mode operations. *For the first time,* excellent RF and mixed-mode performance is demonstrated by the highly integrated RF GCMOS technology. The results show that this technology is most promising for battery-powered system-on-a-chip applications.

INTRODUCTION

Increasing demands for low cost portable wireless communication products in the consumer marketplace, along with the advance in silicon CMOS miniaturization, are the major driving forces behind the development of a silicon-based, CMOS compatible technology for RF mixed-mode applications. The key market drivers for those applications include low cost, high performance, long battery life, and high integration.

Recently, the application of deep-submicron bulk CMOS technology for GHz operation has been reported [1-4]. The RF-GCMOS described here is fully compatible with mainstream CMOS technology, but with improved performance without aggressively pushing the technology through device scaling to reduce cost. The GC-MOSFET is similar to a conventional MOSFET, except that the threshold voltage (Vt) adjust implant in CMOS is replaced by a grade-channel (GC) implant on the source-side only (unilateral). The lateral dopant profiles of the unilateral GCMOS structures are illustrated in Fig. 1 along with the device cross-sections. Compared with the conventional CMOS with uniformly doped channel, channel doping along the surface in the GCMOS is "graded". In a unilateral GCMOS device, the GC implant is confined around source region, the rest of the channel is lightly doped with the same concentration as substrate or well. Similar to a DMOS [5], the device can be viewed as two sub-devices connected in series: an enhancement mode device at the source side, and a depletion mode device at the drain side, each has a different V_t and "channel" length. The "effective" channel length (L_{eff}) when the device is on is mainly determined by the GC region, which is much shorter than the physical gate length. As the result, for the same physical gate length, the GCMOS device can provide higher drive current, higher peak transconductance, higher output resistance, and lower drain junction capacitance than a conventional CMOS device with uniformly doped channel, resulting in a high performance device with high cut-off frequency, high gain and low noise figure, well suitable for RF mixed-mode applications. In addition, the GC implant also effectively suppresses short channel effects and improves drain-to-source punchthrough resistance. Therefore, lightly doped well/substrate can be used to reduce junction capacitance.

RF-GCMOS TECHNOLOGY

The RF-GCMOS technology is based on a low power, low cost GCMOS VLSI technology [6] with the addition of fully integrated passive components and optimized GC-MOSFETs for RF circuit applications. The baseline process consists

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of aggresive-LOCOS isolation, 0.65μm dual-poly gate with 105Å gate oxide, and self-aligned Ti silicide (salicide) in source, drain, and gate regions, and double- or triple-layer metal. The use of salicide reduces parasitic resistance and therefore improves device performance at high frequencies. Since the L_{eff} of a GC-MOSFET is much shorter than the physical gate length, at the same L_{eff}, the physical gate length can be larger than that of a conventional MOSFET, resulting reduced gate resistance. Consequently, improved high frequency performance of a GC-MOSFET can be achieved.

Since this technology uses existing CMOS-based VLSI process technology, it makes it possible to integrate digital, analog, and RF functions onto a single-silicon-chip, therefore opens a door to achieve the ultimate goal of "system-on-a-chip".

DEVICE RESULTS

The superior DC characteristics of GCMOS are compared with CMOS, and the results are summarized in Table 1. More than 30% to 40% saturation current improvement is achieved by GCMOS, with higher g_m, lower body effect, and better drain-induced-barrier-lowering (DIBL) control. Comparisons of the output curves for n-channel devices are shown in Fig. 2. Much improved punchthrough resistance in GCMOS is illustrated in Fig. 3 (similar results were obtained for p-ch device). Clearly, over a range of gate lengths, subthreshold leakage currents of GCMOS remain relatively unchanged, and GCMOS has much lower DIBL than its CMOS counterpart.

Fig.4 shows a typical f_T & f_{max} plot for a n-channel multi-finger RF-GCMOS (W/L=128 μm/0.65μm) at 3 V. Peak f_T of 16 GHz and f_{max} of 22 GHz are achieved. In Fig. 5, noise figure and associated gain of a W/L=256/0.65 (μm/μm) n-channel device at 1.6 GHz and 2.7 V are plotted against drain current. Highly efficient RF power devices are also achieved as shown in the Gain and Efficiency plot (Fig.6) for a 12 mm wide RF-GCMOS power device measured at 3.4 V and 850 MHz. A similar device with 6 mm width achieved 26.5 dBm of output power with 66% efficiency and 11 dB gain, measured at 1.9 GHz and 3.4 V.

CIRCUIT RESULTS

The advantages of this technology for RF mixed-mode applications are further demonstrated using both digital and RF analog circuits. Fig. 7 compares maximum frequency and standby leakage of a SRAM made by GCMOS and CMOS technologies. At 1.8 V, GCMOS is about 20 to 30% faster than CMOS with comparable standby leakage. Similar speed-power advantages are demonstrated using a random logic circuit. Compared with conventional CMOS, improved power-delay performance is demonstrated with the GCMOS technology. As illustrated in Fig. 8, at 1.8V, GCMOS offers about 25-30% lower power-delay product than CMOS. Fully functional RF circuits, such as Integrated Power Amplifiers (IPAs), Low Noise Amplifiers (LNAs), Oscillators (VCOs), Mixers, and Downconverters, etc., have been achieved. As an example, Fig. 9 shows the results of a two-stage IPA measured at 900 MHz and 3.4 V. Output power of more than 30 dBm with 62% PAE was obtained. A LNA designed for 3 V operation at 2 mA obtained 1.4 dB NF with 17 dB gain and -7 dBm input IP3. More detailed circuit results will be reported later [7].

CONCLUSION

In conclusion, a CMOS-compatible RF-GCMOS IC technology has been developed to provide a low cost, mixed-mode, and highly integrated solution to wireless communication applications. The advantages of the technology for those applications have been demonstrated *for the first time* on both digital and RF analog circuits. The results show that the technology is most promising for battery-powered system-on-a-chip applications.

ACKNOWLEDGMENTS

The authors would like to thank Motorola ACT Process & Integrated Development Fab for wafer processing support, and to Dr. Ken Papworth for VLSI test support.

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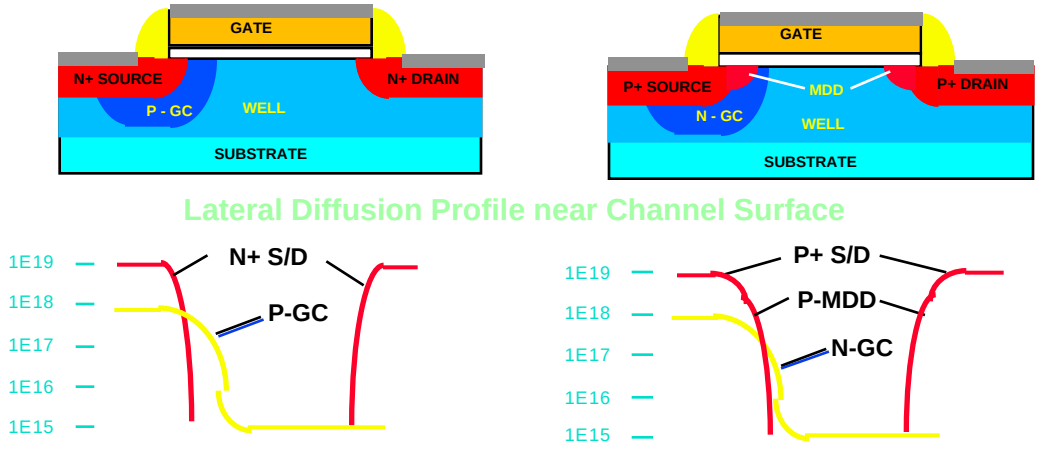

Figure 1 Cross-section views of the unilateral GCMOS - N-channel (left) and P-channel (right). Also shown are lateral diffusion profiles in the channel near the Si/SiO2 interface.

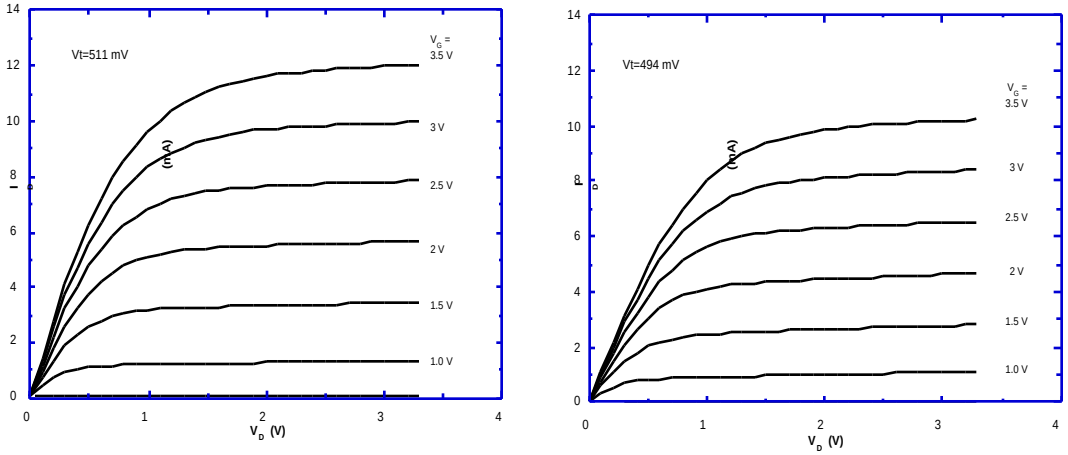

Fig. 2 Output characteristics for (left) n-channel GCMOS and (right) conventional n-channel MOS transistors with W/L =24µm/0.6µm.

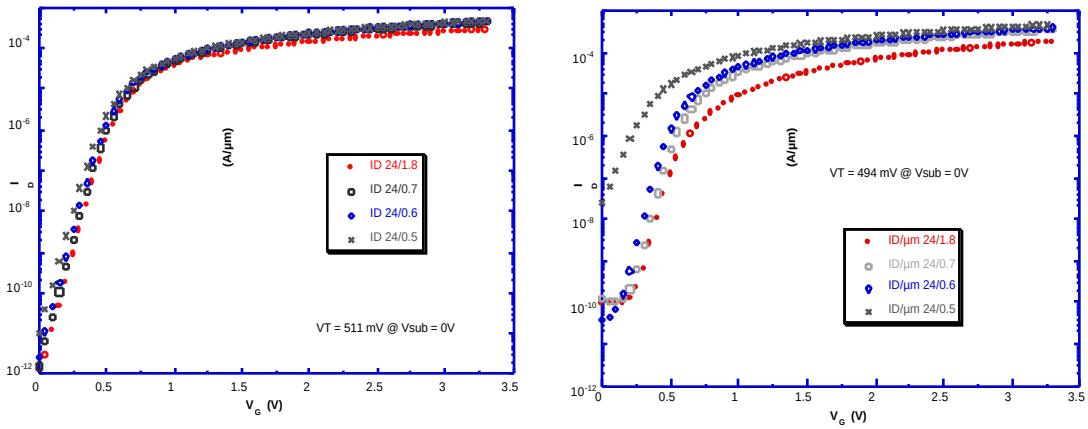

Fig. 3 Subthreshold characteristics for 24µm wide devices at Vd=2.5V as a function of gate length for (left) n-channel GCMOS and (right) conventional n-channel MOS transistors.

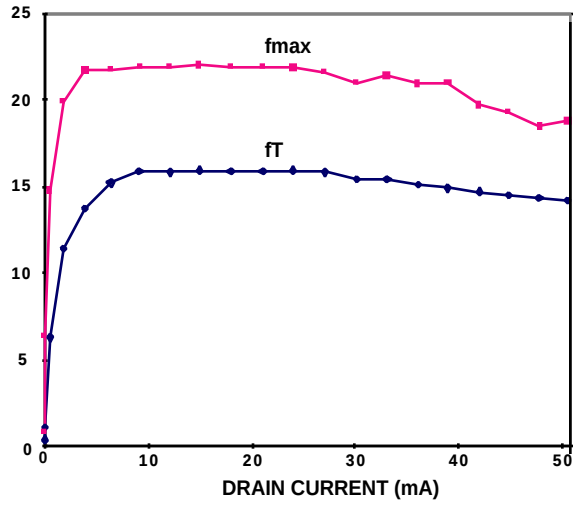

Fig. 4 fT and fmax of a 128µm wide n-ch RFGCMOS at 3.0V.

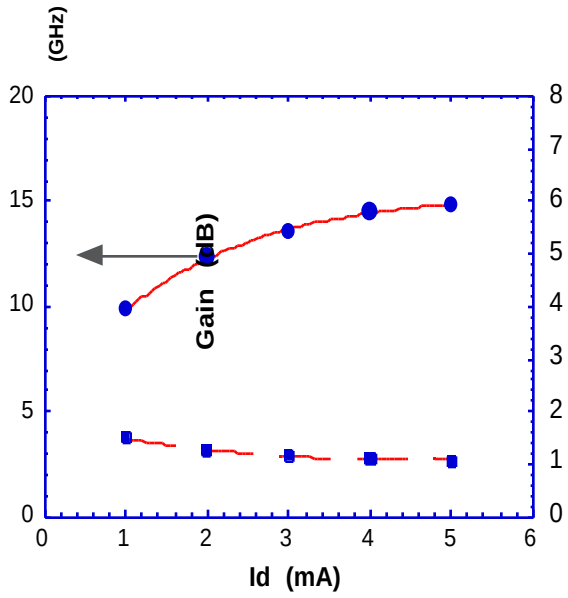

Fig. 5 NF and Gain of a 256µm wide n-ch RFGCMOS device.

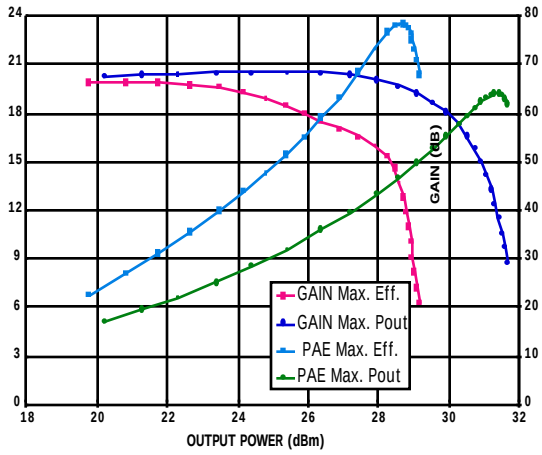

Fig. 6 Gain and Eff. plot for a 12mm wide power device CMOS. at 3.4V and 850MHz.

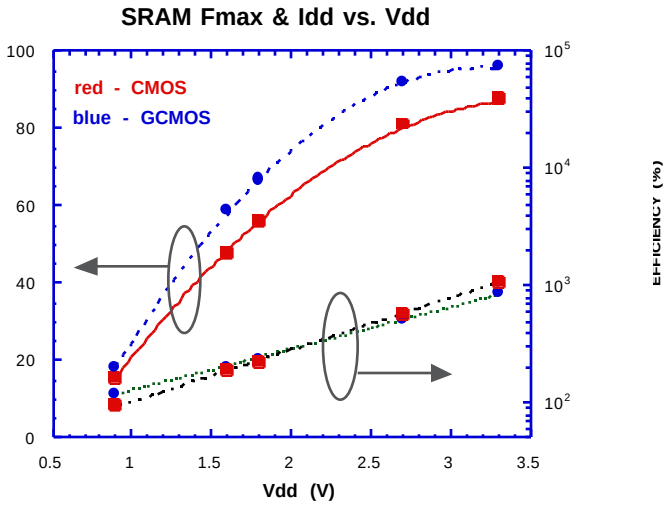

Fig.7 SRAM fmax and Iddq Comparison: GCMOS vs.

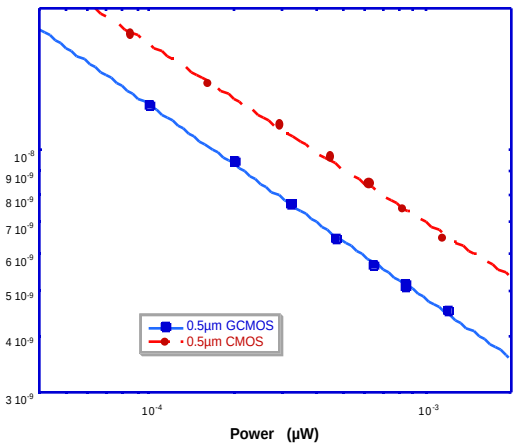

Fig. 8 Logic block power-delay trade-off comparison

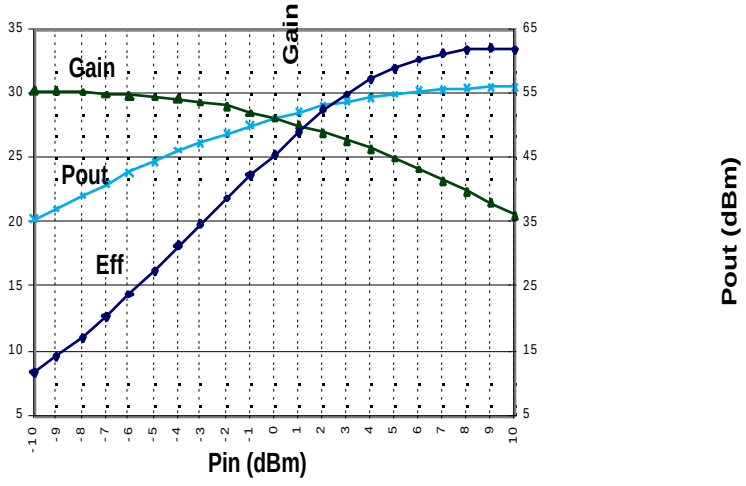

Fig. 9 Results from a 2-stage IPA at 900MHz and 3.4V.

Table I. Key DC device parameter comparison at Vd=1.2V

Key Parameter	N-GCMOS	N-CMOS	P-GCMOS	P-CMOS
Vt (mV)	494	490	471	495
gm (µS/µm)	37	23	9.8	7.6
Idsat (µA/µm)	82	53	26	19
Body Effect (mV)	57	206	200	225
DIBL (mV/V)	16	22	12	19
Idss (pA/µm)	2	1.1	0.5	0.6
Ss (mV/dec)	81	80	84	81
Leff (µm)	0.51*	0.52	0.4*	0.45
BVdss@1nA (V)	5.4	9	8	8.4

(*Leff for GCMOS measured on “natural” devices without GC implant)

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